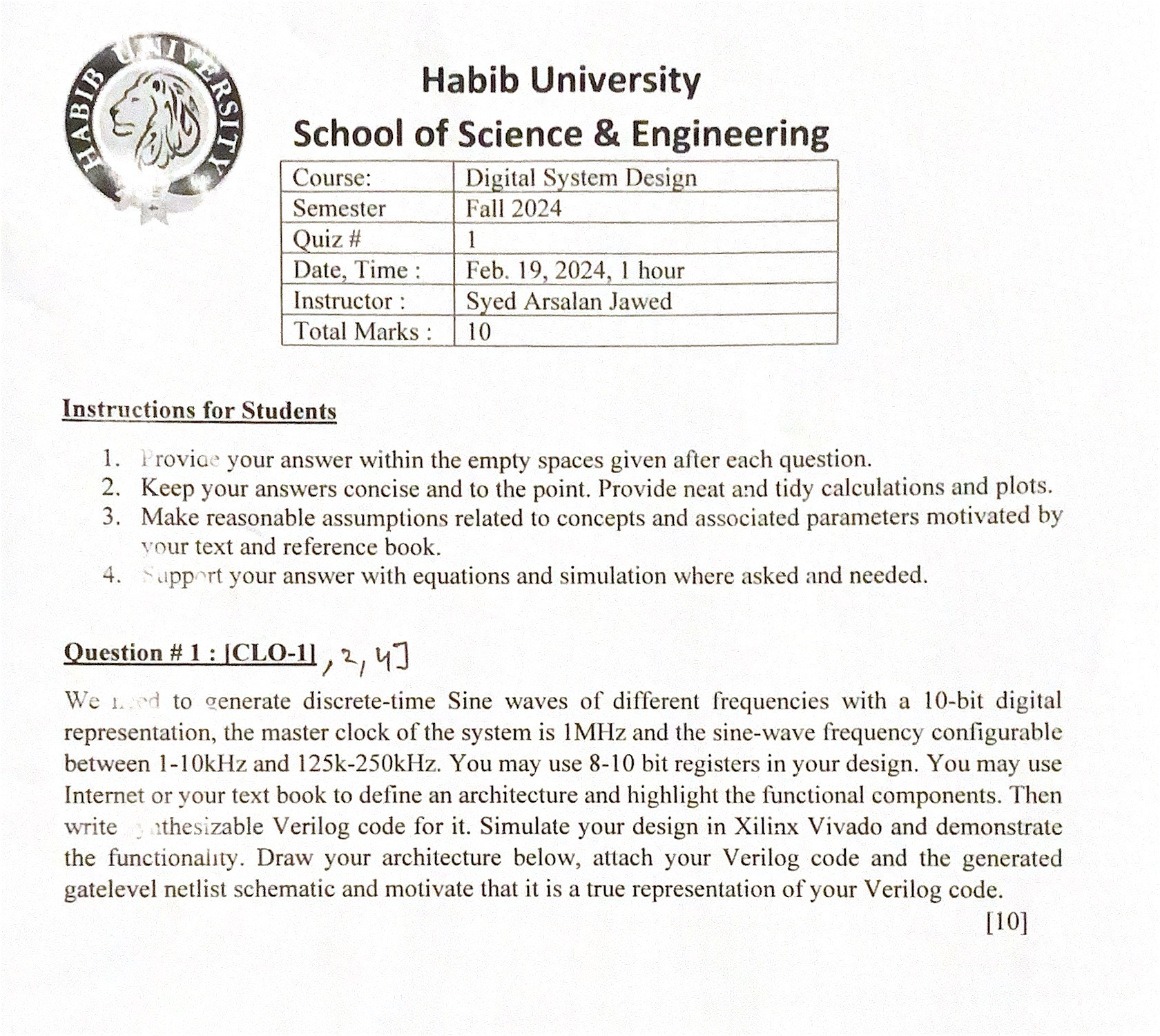
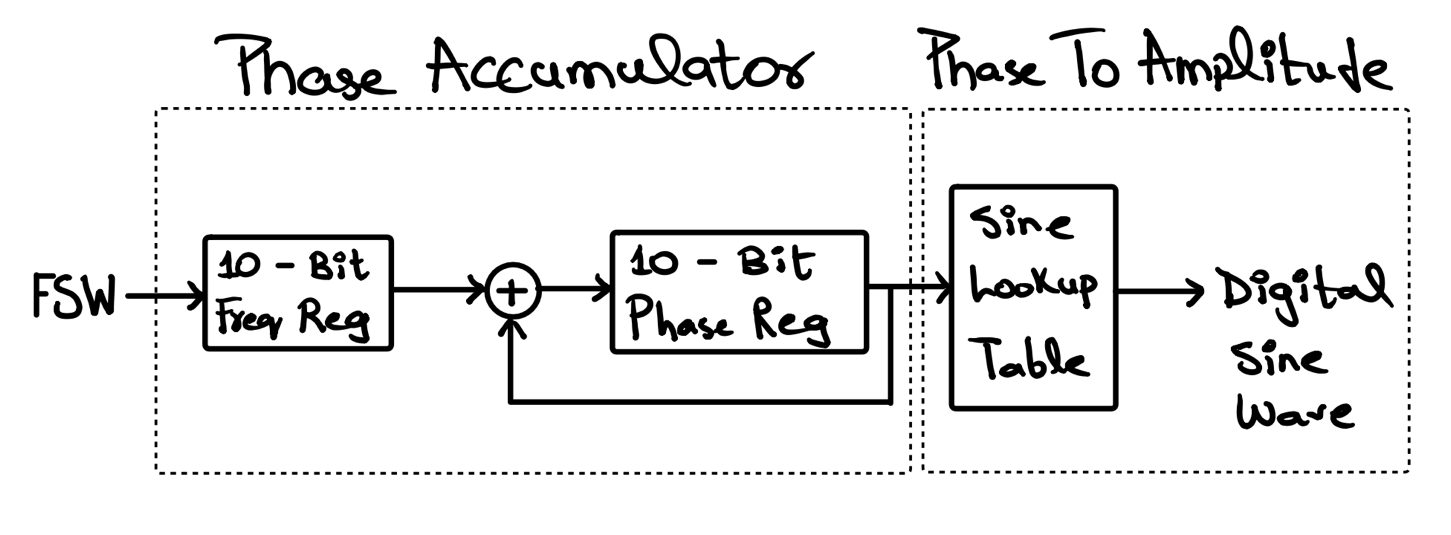
Name: Huzaifah Tariq Ahmed HUID: ha07151

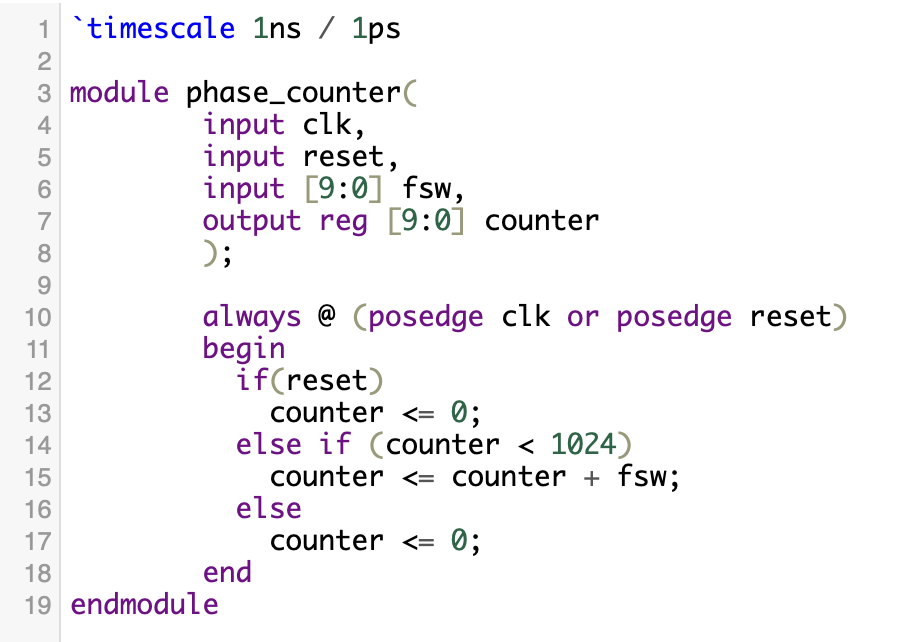


Proposed Architecture:



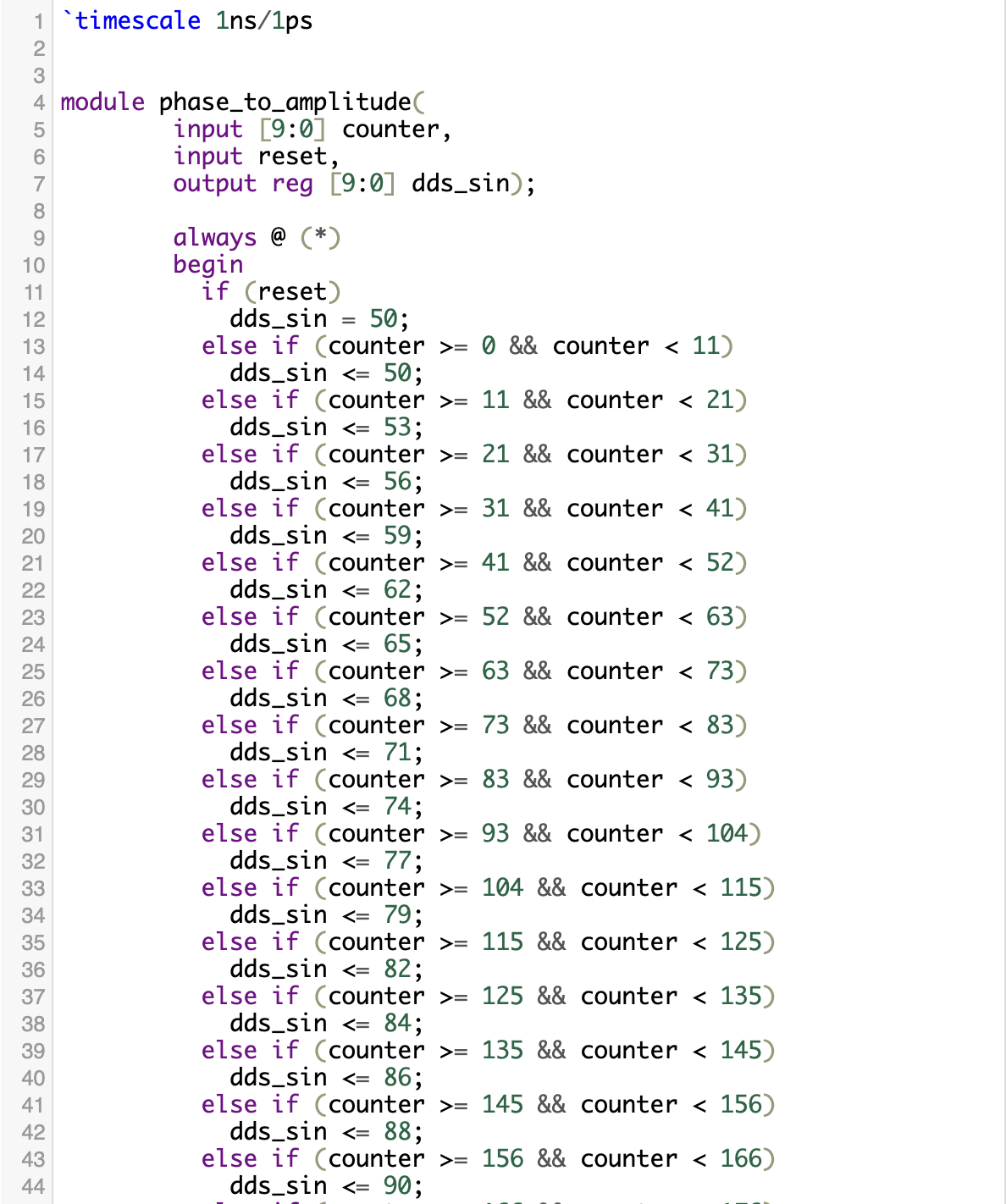
Phase Accumulator:

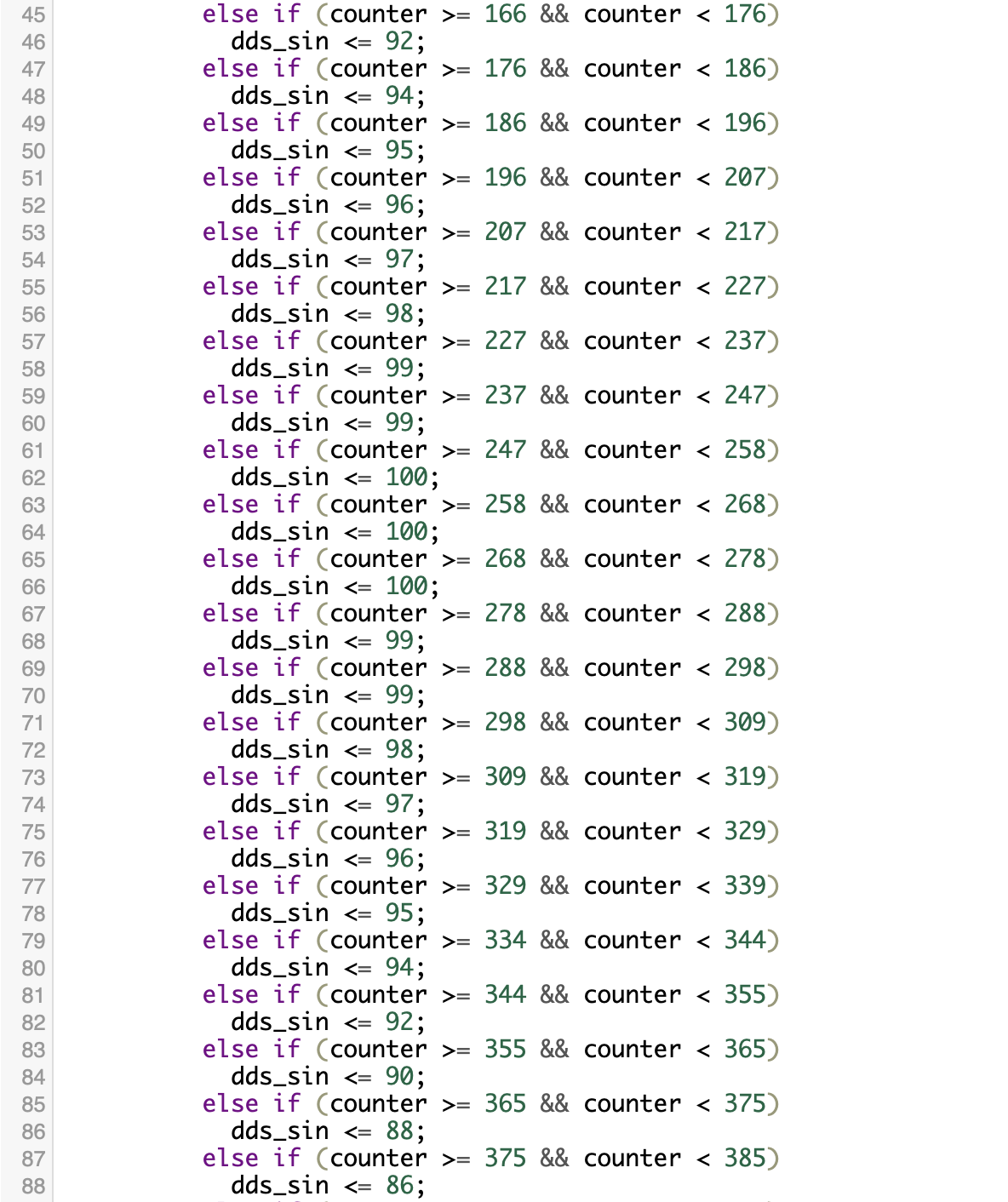
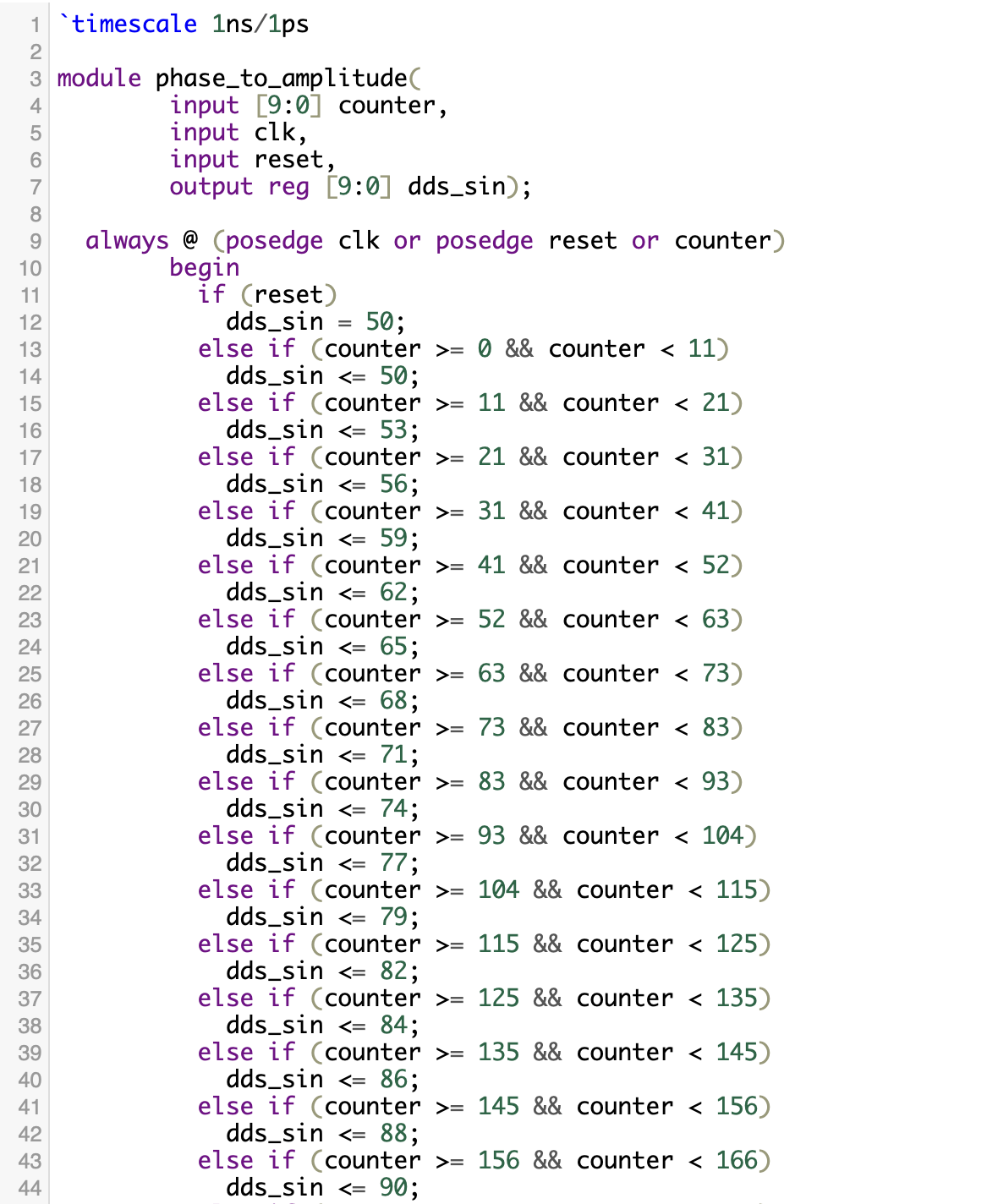
Code:

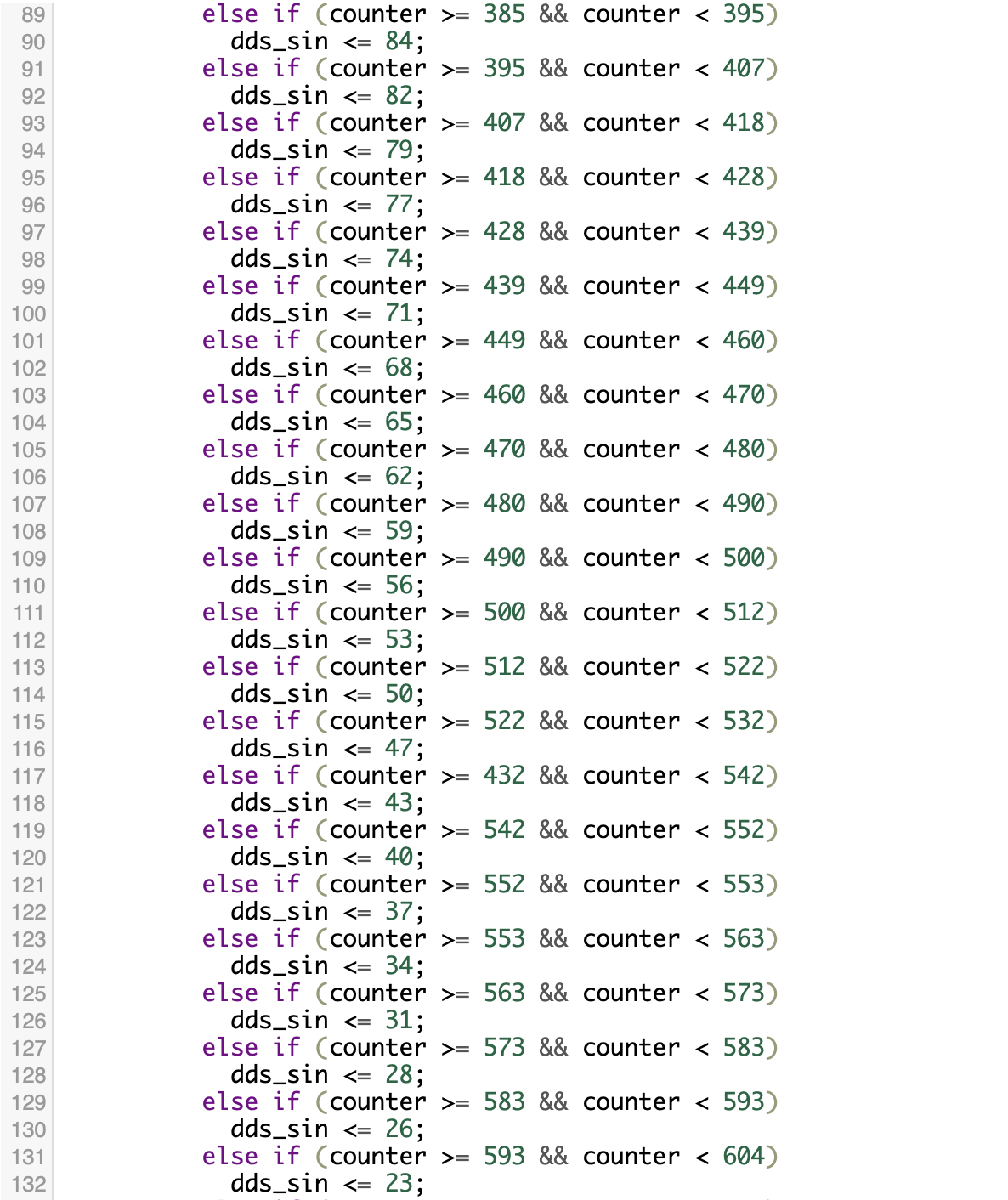
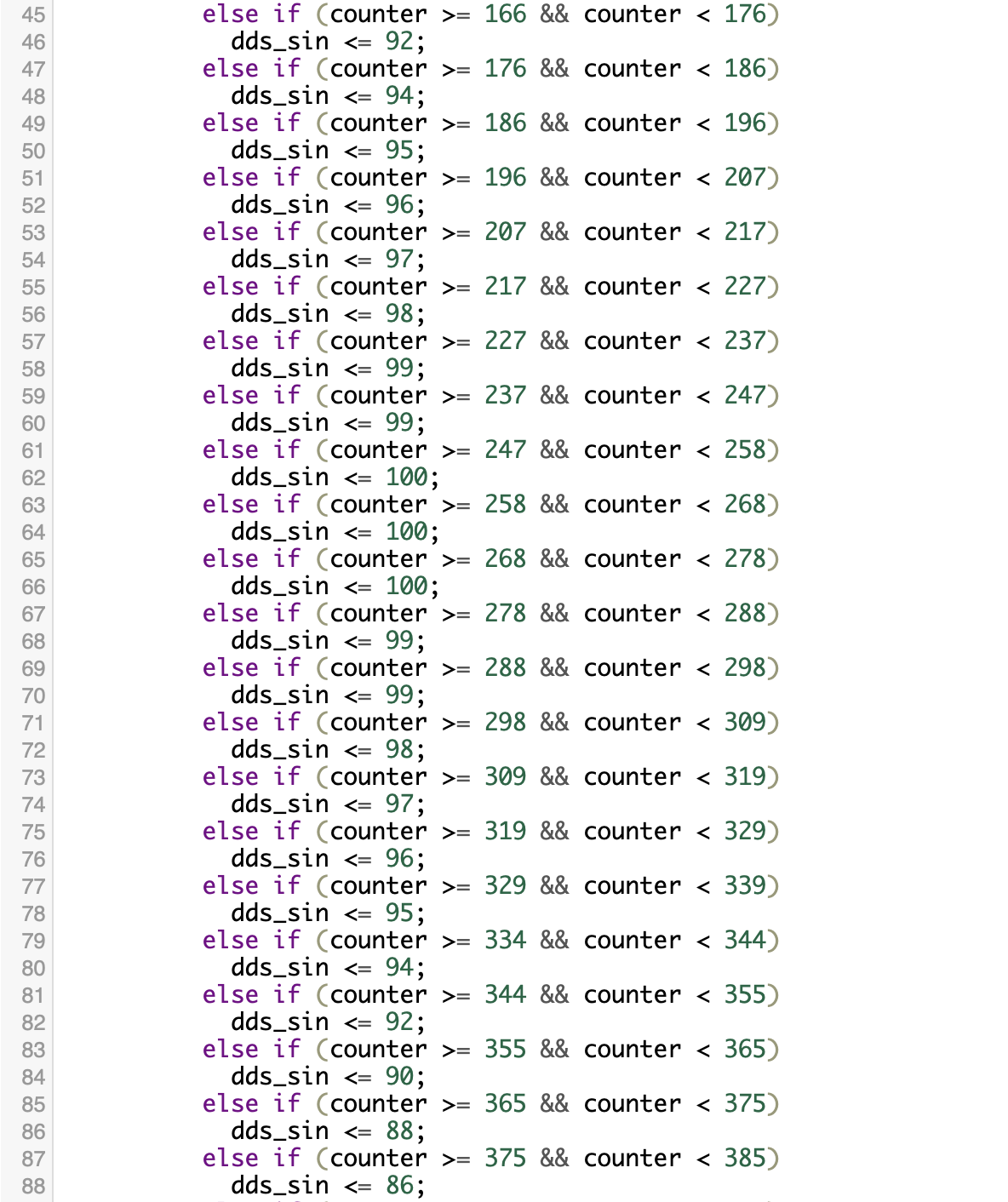


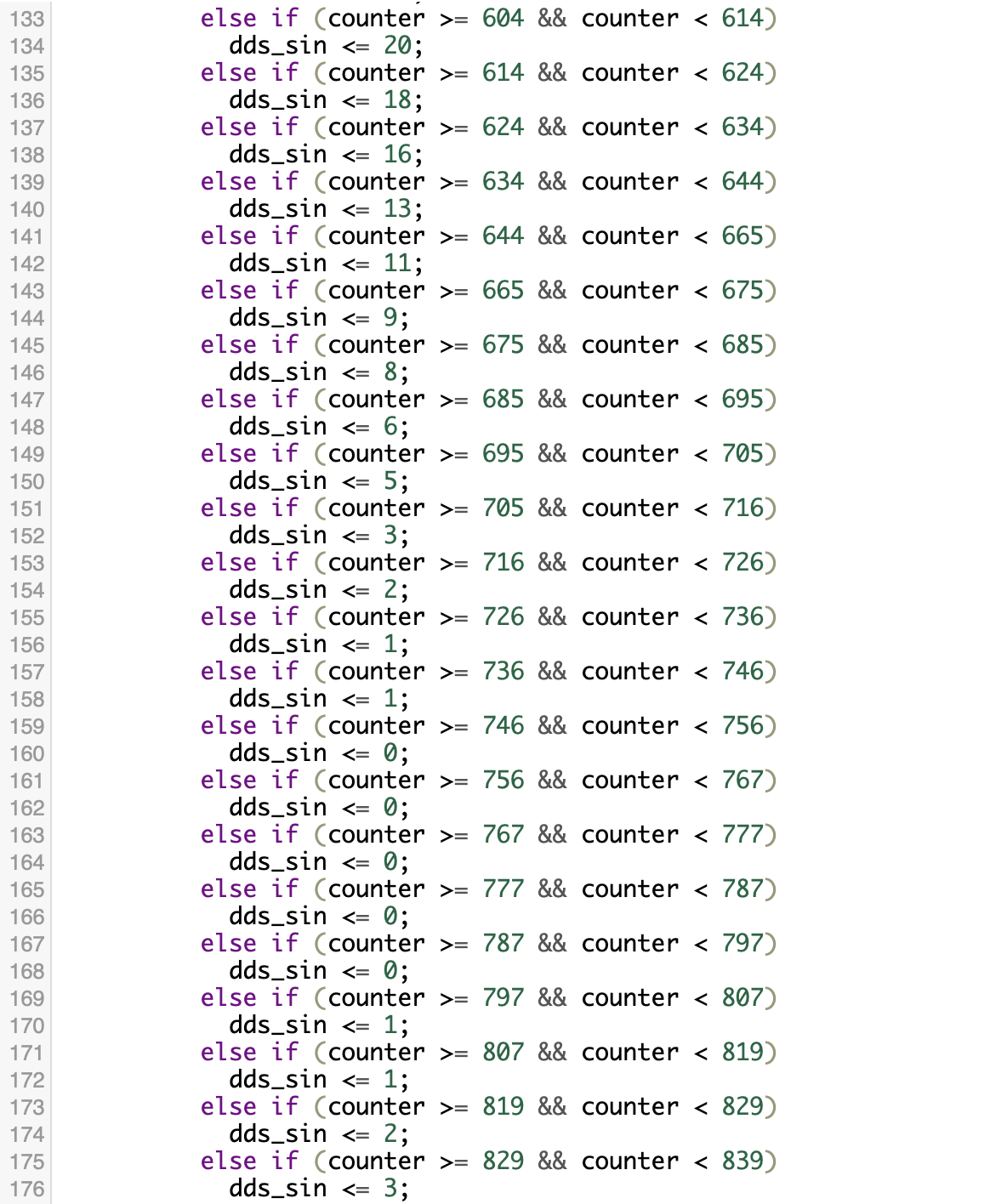
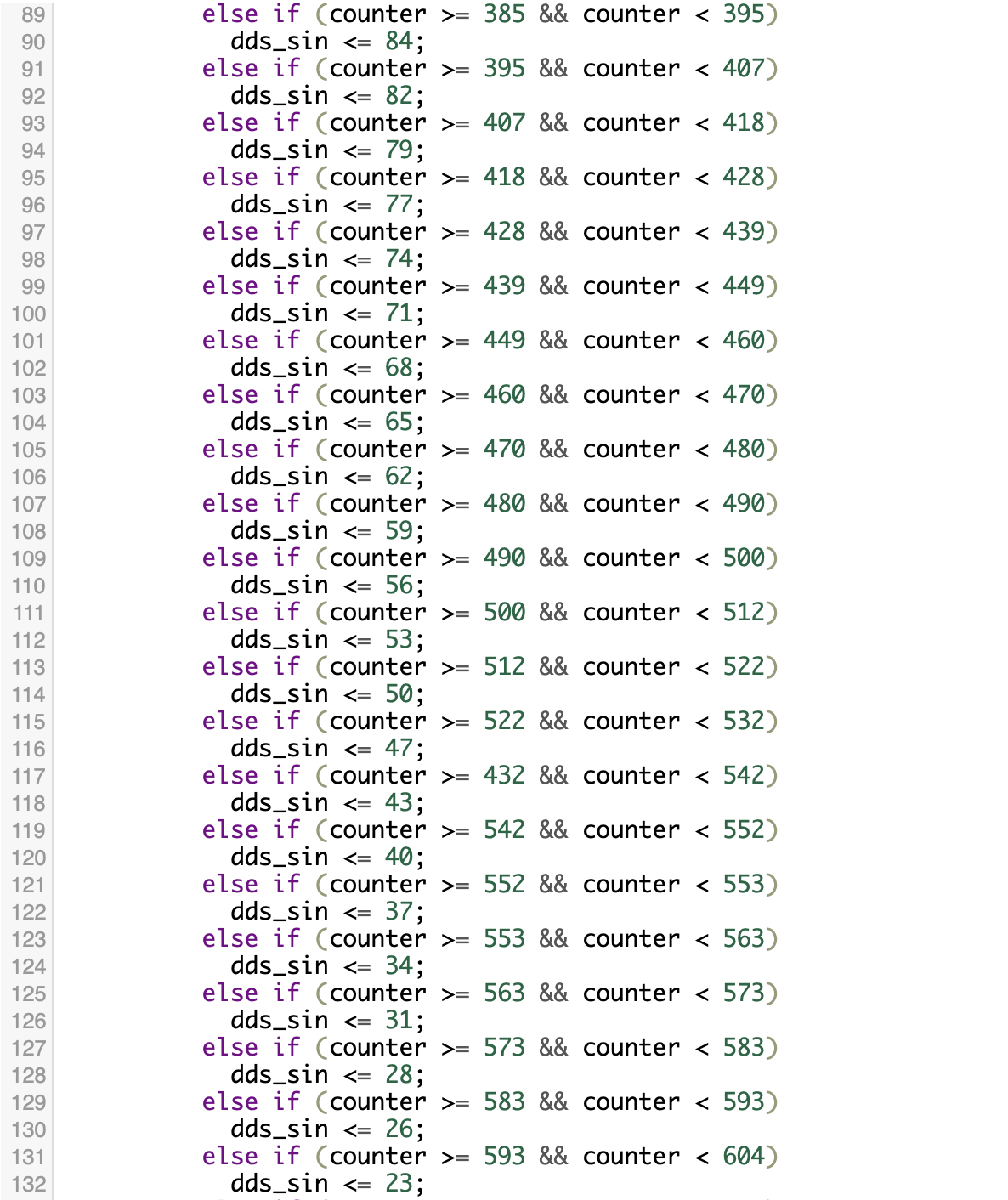
Phase To Amplitude:

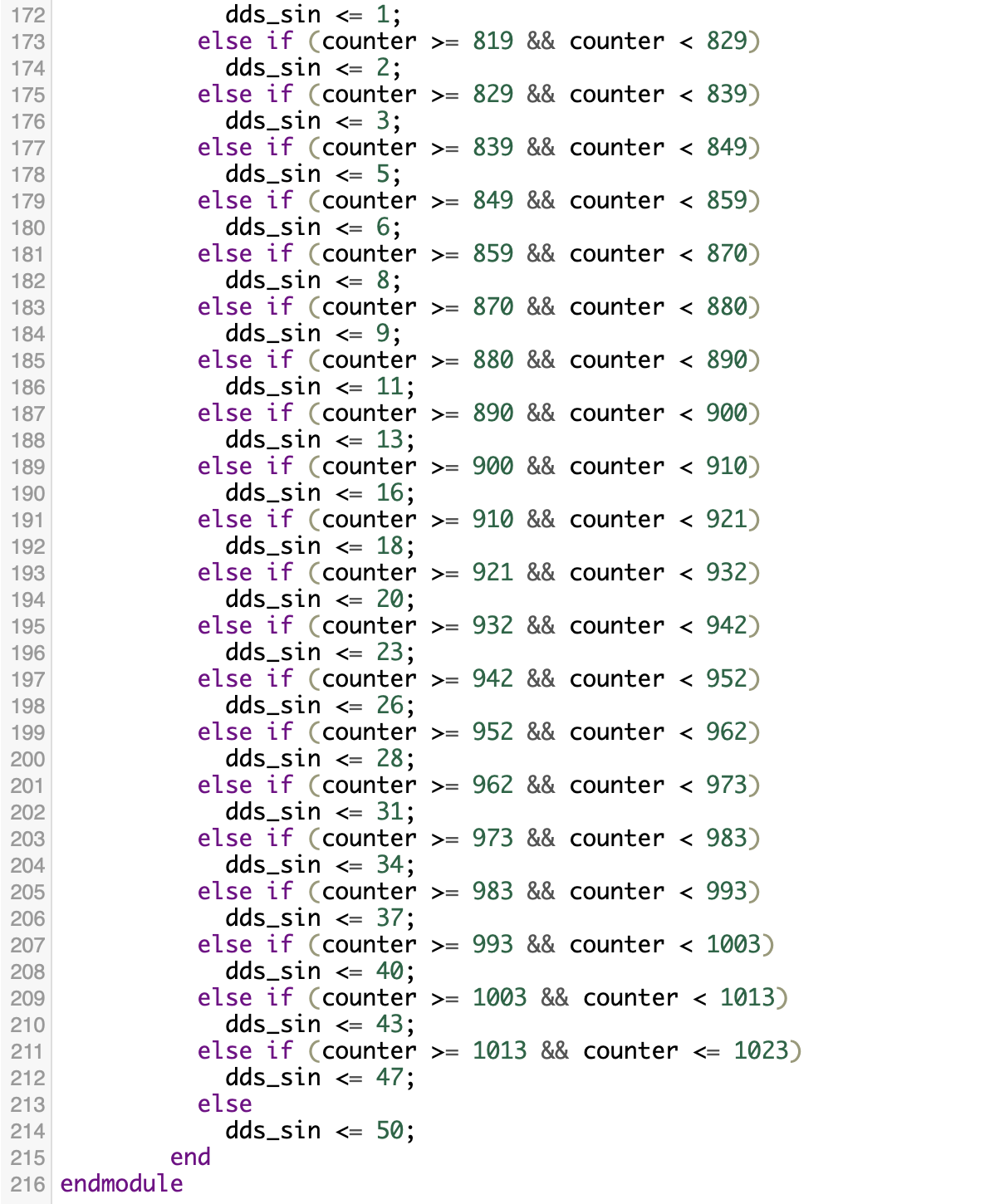
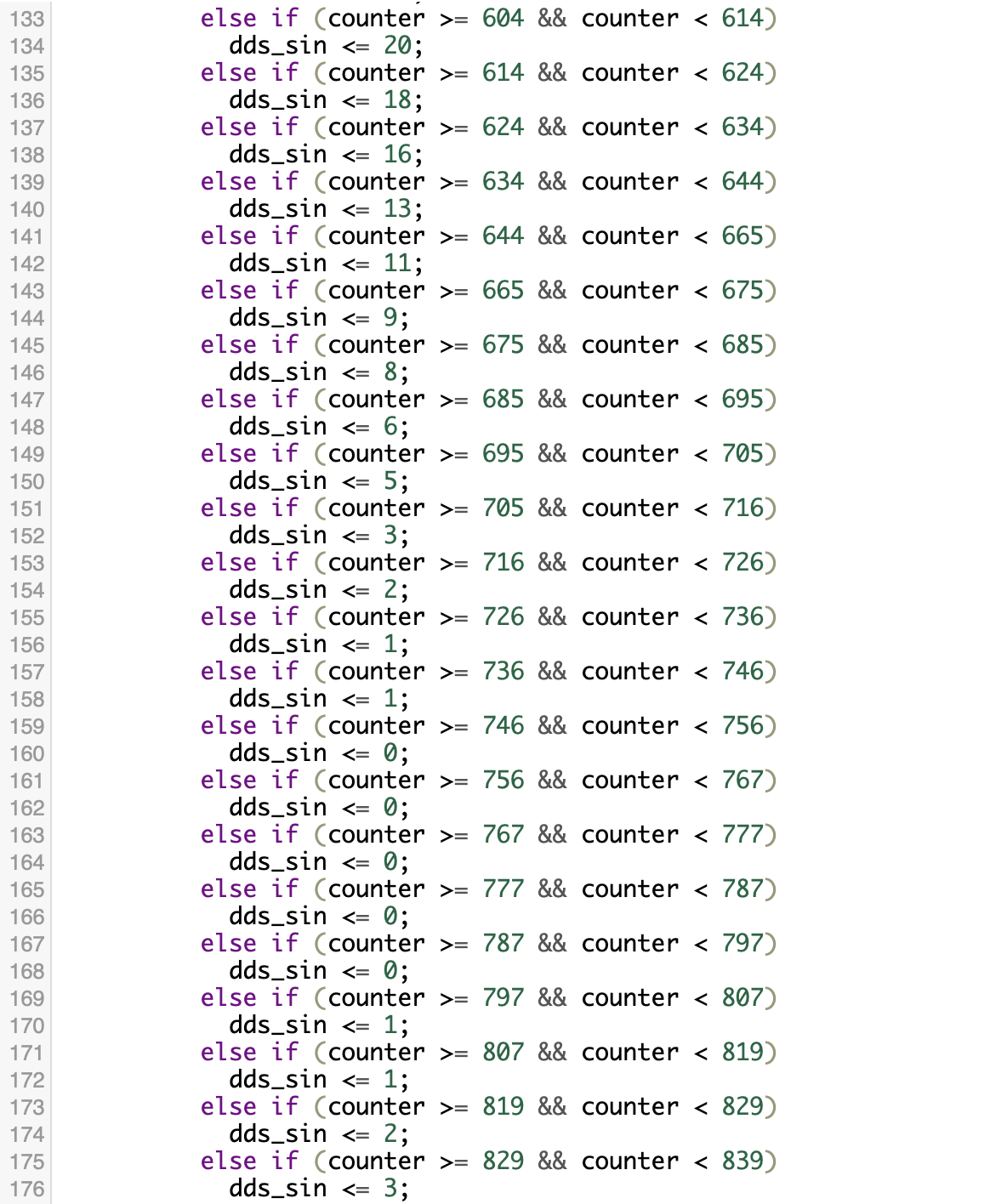
Code:

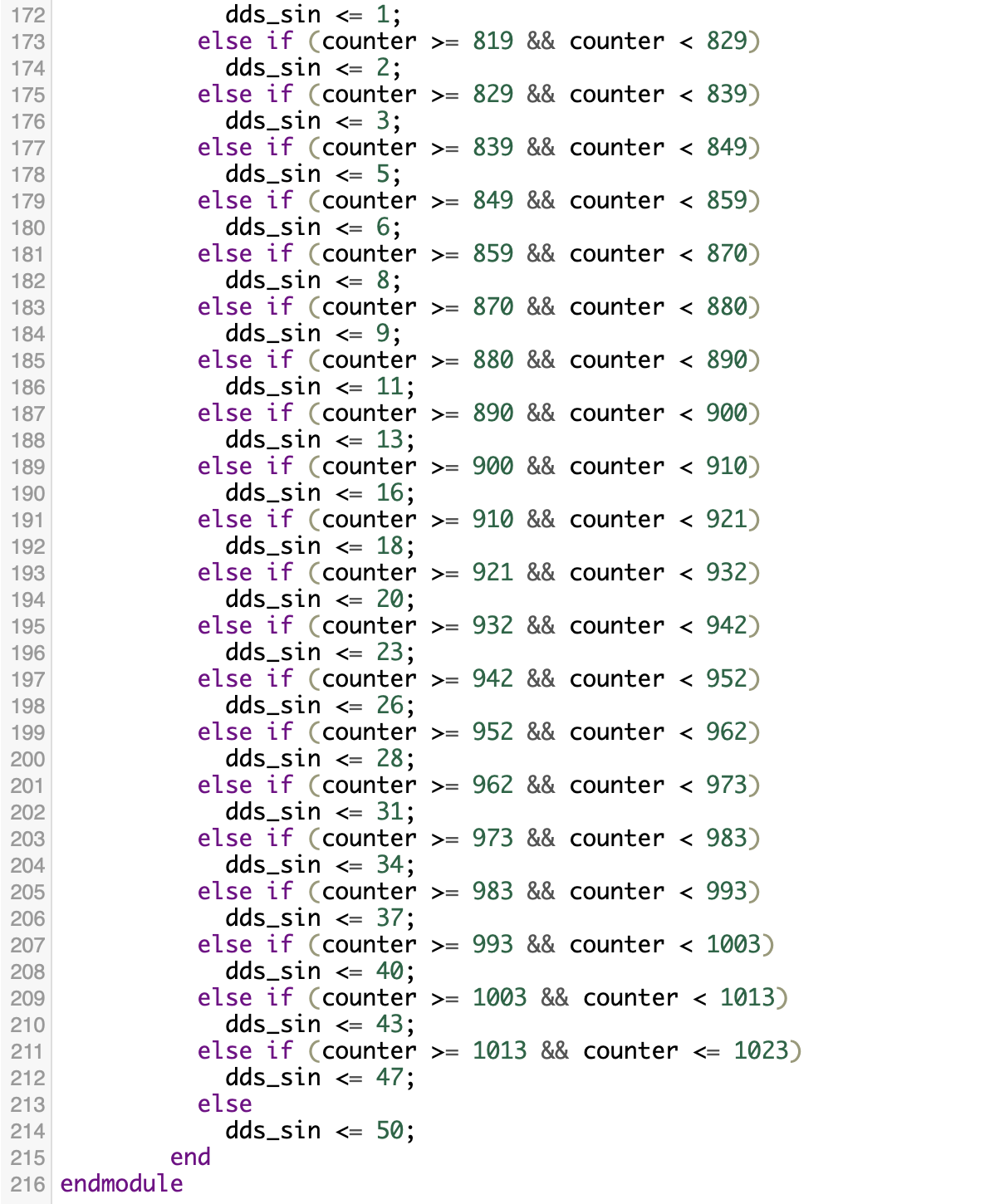






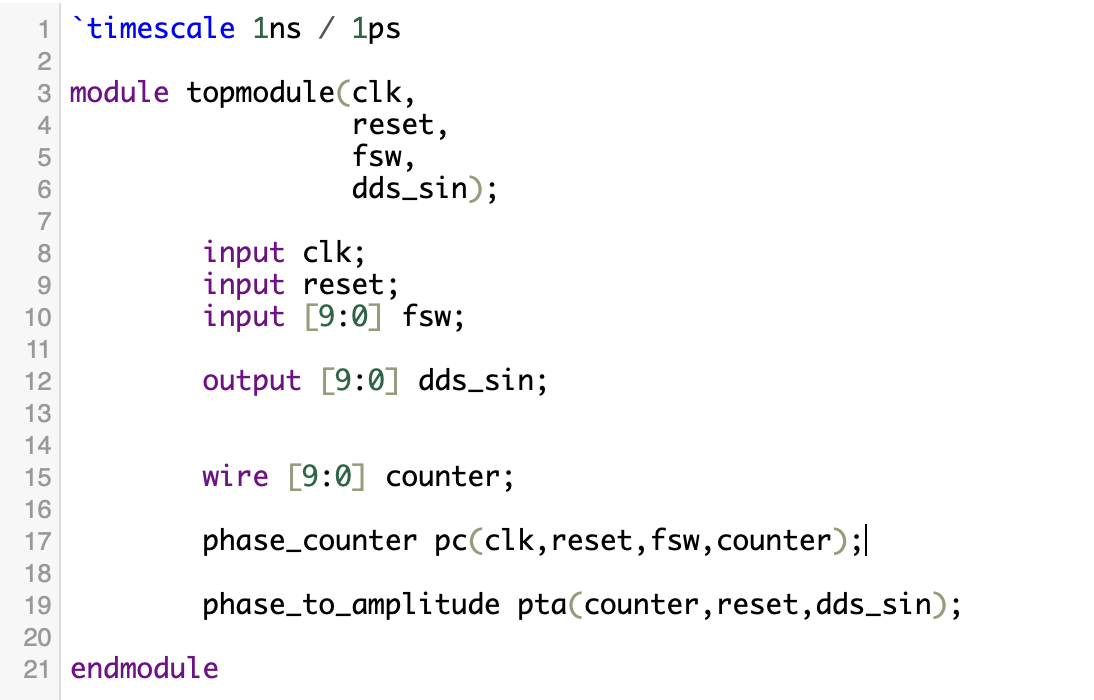






Top Module:

Code:



Schematic:

A computer program with a computer program

Description automatically generated with medium confidence

As you can see this Vivado Schematic is pretty much same as what was originally proposed. You can see a 10 bit fsw going into phase counter which is our phase accumulator and then the counter value going to phase to amplitude block where it assigns a specific amplitude to that counter value, giving us a digital sine wave as output.

Testbench:

